REMARKS

This amendment is being filed as a response to the Final Office Action of October 19,

2007. Reconsideration is respectfully requested in view of these clarifying amendments and

remarks.

Objections to the Specification

The Office has objected to the specification. Applicant respectfully asserts that such

objections are rendered moot in view of the amendments submitted hereinabove.

Rejections under 35 USC § 103(a)

Claims 1-4, 10-12, 14, 16, 17, 22, 24-27, 29, 31, and 33-37 have been rejected under

35 U.S.C. 103(a) as being unpatentable over Tetrick (US Patent No. 6,003,112), in view of

Fujihira et al. (U.S. Patent No. 5,278,965). This rejection is respectfully traversed.

Applicants respectfully request reconsideration of these rejections in light of the arguments

contained herein.

Independent Claims 1, 22, and 31 were rejected as allegedly being obvious over

Tetrick in view of Fujihara et al. Applicants traverse this rejection, because there is no

motivation or suggestion to combine the teachings of Tetrick with Fujihara et al. to provide

the claimed invention. Applicant's arguments made in the Amendment filed August 7, 2007

are hereby incorporated by reference.

In the Response to Arguments Section, the Office has asserted that "it would be

obvious to one having ordinary skill in the art to modify the memory controller and method

for copying data from a first memory location to a second memory location which defers

write cycles to a second memory location when copying data between a first and a second

memory location as taught by Tetrick, and instead terminate the transmission of the data to

the second random access memory location, during transmission of the quantity thereto, in

response to the processor generating a write request to the second random access memory

location as taught by Fujihira as Fujihira explicitly discloses." The Examiner's comments are

respectfully traversed as the references are not combinable because the references teach away

from their combination.

Furthermore, independent Claims 1, 22, and 31 define wherein said command

specifies said first and second random access memory locations, with the first controller

monitoring operation of the processor to terminate the transmission of the data to the second

random access memory location, during transmission of the quantity thereto, in response to

the processor generating a <u>write request to the second random memory location</u> (see this or

similar, but not necessarily identical language in the independent claims). The Office has

asserted that Fuhijira discloses the aforementioned limitation, and has quoted that "during the

DMA transfer <u>between two memories</u>, it is possible to make a normal interruption of the

DMA transfer as if the interrupt request signal DONE is generated, by <u>making a write</u>

<u>operation with respect to the register 18</u> from the CPU 50" (Col. 6, lines 13-21 - emphasis

added). Applicant respectfully disagrees.

Fuhijira teaches to interrupt the memory transfer by making a write operation to a

register 18 in the data handler (see Fig. 3). Register 18 is not part of memory, and it is not the

destination address for the memory transfer. Applicant claims terminating the transmission

of data when the processor generates a write request <u>to the second memory location</u>, and not

to a register, as in Fuhijira. Therefore, terminating the data transmission by making a write

operation to a register, as in Fuhijire, does not suggest terminating the data transmission when

the processor generates a write request to the second memory address from the memory transfer request, as claimed.

Independent Claims 1 and 22, now incorporating the subject matter from former Claims 3 and 24, describe that the data is copied from the first random access memory location to the second random access memory location by an internal memory transfer, without traveling over the data communications facility. The Office has asserted that Tetrick teaches the aforementioned limitation in Col. 3, lines 4-7, and Col. 6, lines 35-38. Applicant respectfully disagrees.

Tetrick merely teaches that "the memory interface 150 operates to copy a data structure from a first location in the memory 113 to a second location in the memory 113 when a memory-to-memory copy is requested" (Col. 3, lines 4-7), and that "memory copy operation can copy the data structure at the first location in memory to the second location in memory using any known techniques" (Col. 6, lines 35-38 - emphasis added). Tetrick does not teach a memory transfer where the data does not travel over the data communications facility (aka bus). Applicant asserts that transferring data without traveling over the data communications facility was not a known technique at the time, therefore Tetrick does not suggest the incorporated subject matter from former Claims 3 and 24.

Additionally, it appears that the Examiner has relied on an inherency argument regarding the above emphasized claim limitations. In view of the arguments made hereinabove, any such inherency argument has been adequately rebutted, and a notice of allowance or a specific prior art showing of such claim features, in combination with the remaining claim elements is respectfully requested (See MPEP 2112).

Further, in response, applicant asserts that the fact that a certain result or characteristic may occur or be present in the prior art is not sufficient to establish the inherency of that result or characteristic. In re Rijckaert, 9 F.3d 1531, 1534, 28 USPQ2d 1955, 1957 (Fed. Cir. 1993); In re Oelrich, 666 F.2d 578, 581-82, 212 USPQ 323, 326 (CCPA 1981). "To establish inherency, the extrinsic evidence 'must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill. Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient.'" In re Robertson, 169 F.3d 743, 745, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999).

Claims 20 and 39 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Tetrick and Fujihira et al., and further in view of Garret et al. (U.S. Patent No. 6,408,369). This rejection is respectfully traversed. Applicants respectfully request reconsideration of these rejections in light of the arguments contained herein.

Claims 20 and 39 define that said first controller transmits an acknowledgement of said command back to the processor, and that the processor is responsive to a failure to receive said acknowledgement within a predetermined time-out period to perform said copy operation by issuing separate read and write commands. The Office has relied on Garret to suggest the aforementioned limitations. Applicant respectfully disagree.

Garret teaches that 'the controller returns a "command not completed" back to the host computer and the host computer can either try the operation again, or transfer the data using a prior art command sequence' (Col. 3, line 67 - Col. 4, line 3). However, Garret host always waits for the status, "command not completed" in this case, to proceed. There is no suggestion in Garret that the host will proceed after a failure to receive said

acknowledgement within a predetermined <u>time-out period</u>. Therefore, a system that waits for

a status result, as in Garret, does not suggest a system that proceeds after a predetermined

time-out period, as claimed.

      In view of the foregoing, the Office is requested to withdraw the rejection of claims 1,

20, 22, 31, and 39 under §103. The dependent claims are submitted to be patentable for at

least the same reasons the independent claims are believed to be patentable. The Applicants

therefore respectfully request reconsideration and allowance of the pending claims. A Notice

of Allowance is respectfully requested.

      If the Examiner has any questions concerning the present amendment, the Examiner is

kindly requested to contact the undersigned at (408) 774-6920. If any other fees are due in

connection with filing this amendment, the Commissioner is also authorized to charge

Deposit Account No. 50-0805 (Order No. SUNMP438). A duplicate copy of the transmittal

is enclosed for this purpose.

                                 Respectfully submitted,
MARTINE PENILLA & GENCARELLA, LLP

/Jose M. Nunez/

Jose M. Nunez
Reg. No. 59,979

710 Lakeway Drive, Suite 200
Sunnyvale, CA 94085
Telephone: (408) 749-6900
Facsimile: (408) 749-6901